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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,021	02/25/2004	Kouichi Matsushita		9033

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MATTINGLY, STANGER & MALUR, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

EXAMINER	
CHOE, HENRY	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 08/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,021	MATSUSHITA ET AL.	
	Examiner	Art Unit	
	Henry K Choe	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/25/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liwinski (Fig. 1).

Regarding claim 11, Liwinski (Fig. 1) discloses an amplifier circuit comprising a first power transistor (Q2), a first capacitor (C1) having a first terminal (upper terminal of C1) and a second terminal (bottom terminal of C1) which is coupled to the input terminal (the terminal where the RF in signal is receiving) of the first power transistor (Q2), and a bias circuit (BIAS CIRCUIT) which includes a first transistor (Q1) and a first circuit (Q3) and wherein the first transistor (Q1) being configured as to form a current mirror circuit with the first power transistor (Q2) and the first circuit (Q3) receiving a control signal (Vreg) and providing to the first transistor (Q1) a current signal (Icm) according to the control signal (Vreg). As described above, Liwinski (Fig. 1) discloses all the limitations in the claim 11 except for that the first power transistor being formed on a semiconductor chip.

It is well known to integrate the electronic circuits in the semiconductor chip in order to form of small sized Integrated Circuit (IC). Therefore, it would have been obvious to have integrated the first power transistor of Liwinski (Fig. 1) in the semiconductor chip because such a modification would have advantageously produced a small-sized integrated circuit.

Regarding claim 12, the first transistor (Q1) is a bipolar transistor which is configured as a diode with the input terminal (base terminal of Q1) of the first transistor (Q1) coupled to the first terminal (collector terminal of Q1) of the first transistor (Q1) and wherein the current signal (Icm) is provided to the first terminal (collector terminal of Q1) of the first transistor (Q1). As described above, Liwinski (Fig. 1) discloses all the limitations in the claim 12, except for that the first transistor (Q1) being a FET. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted well known art-recognized equivalent transistors such as a FET in place of the bipolar transistor in the circuit of the Liwinski (Fig. 1) because such a modification would have been considered a mere substitution of art-recognized equivalent transistors.

Regarding claim 13, the input terminal (base terminal of Q2) of the first power transistor (Q2) is coupled to the input terminal (base terminal of Q1) of the first transistor (Q1).

Regarding claim 14, Liwinski (Fig. 1) discloses all the limitations in the claim 14, except for that the first power transistor (Q2) being a FET. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted well known art-recognized equivalent transistors such as a FET in place of the bipolar transistor in the circuit of the Liwinski (Fig. 1) because such a modification would have been considered a mere substitution of art-recognized equivalent transistors.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.

HENRY CHOE
PRIMARY EXAMINER

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